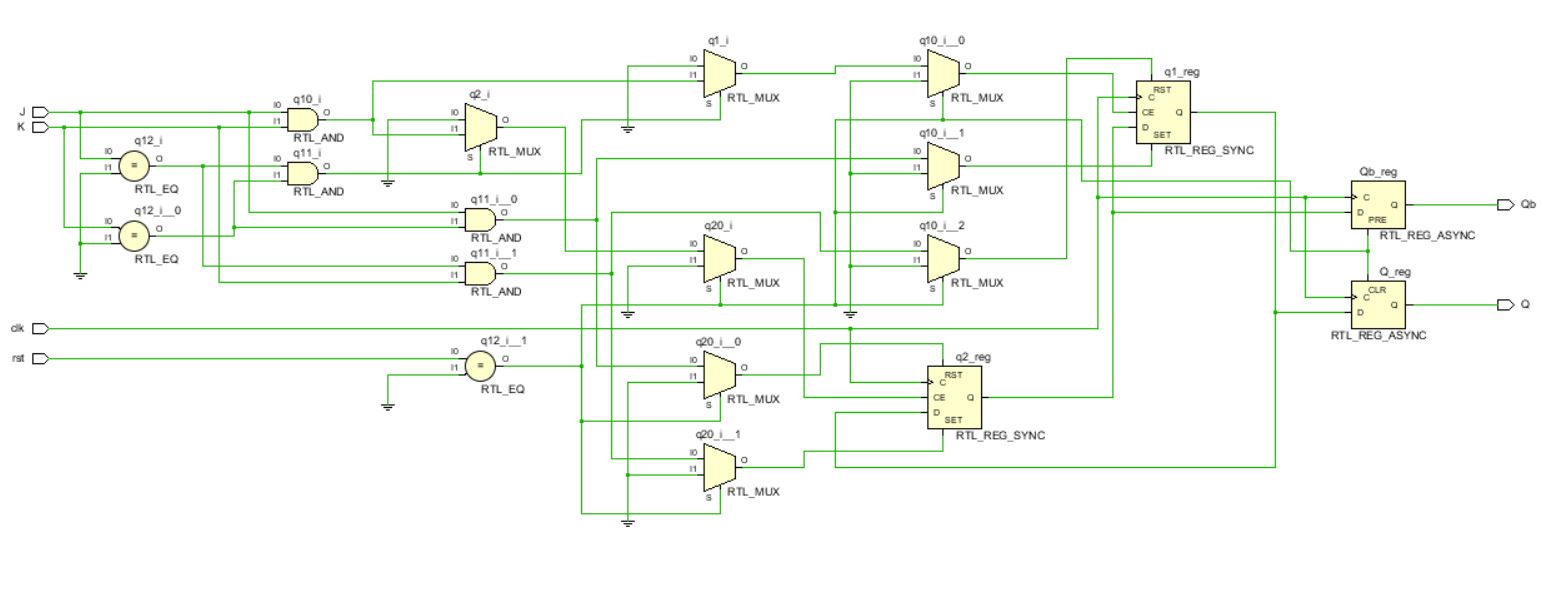
**Practical 5**

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| --- | --- | --- | --- |
| |  |  |  | | --- | --- | --- | | |  |  | | --- | --- | | |  | | --- | | **Aim:** Write a VHDL Code to implement JK Flipflop | | |   **Code:**  library IEEE;  use IEEE.STD\_LOGIC\_1164.ALL;  entity JK\_FF is  Port ( clk : in STD\_LOGIC;  rst : in STD\_LOGIC;  J : in STD\_LOGIC;  K : in STD\_LOGIC;  Q : out STD\_LOGIC;  Qb : out STD\_LOGIC);  end JK\_FF;  architecture Behavioral of JK\_FF is  signal q1:std\_logic:='0';  signal q2:std\_logic:='1';  begin    process(rst,clk,J,K)  begin  if (rst='0') then  Q<='0';  Qb<='1';  elsif(rising\_edge(clk)) then  if(J = '1' and K = '0')then  q1<='1';  q2<='0';  elsif(J = '0' and K = '1') then  q1<='0';  q2<='1';  elsif(J = '0' and K = '0') then  q1<= q1;  q2<=q2;  elsif(J ='1' and K ='1') then  q1<= q2;  q2<= q1;  end if;  Q<=q1;  Qb<=q2;  end if;  end process;    end Behavioral; |
|  |

**RTL DIAGRAM:**

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**Test bench Code :**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity Tb\_JK\_FF is

-- Port ( );

end Tb\_JK\_FF;

architecture Behavioral of Tb\_JK\_FF is

component JK\_FF is

Port ( clk : in STD\_LOGIC;

rst : in STD\_LOGIC;

J : in STD\_LOGIC;

K : in STD\_LOGIC;

Q : out STD\_LOGIC;

Qb : out STD\_LOGIC);

end component JK\_FF;

signal clk,rst,J,K,Q,Qb:std\_logic;

begin

x1:JK\_FF port map(clk,rst,J,K,Q,Qb);

process

begin

clk<='1';

wait for 4ns;

clk<='0';

wait for 4ns;

end process;

process

begin

rst<='0';

wait for 10ns;

rst<='1';

J<='0';

K<='0';

wait for 10ns;

J<='1';

K<='0';

wait for 10ns;

J<='0';

K<='1';

wait for 10ns;

J<='1';

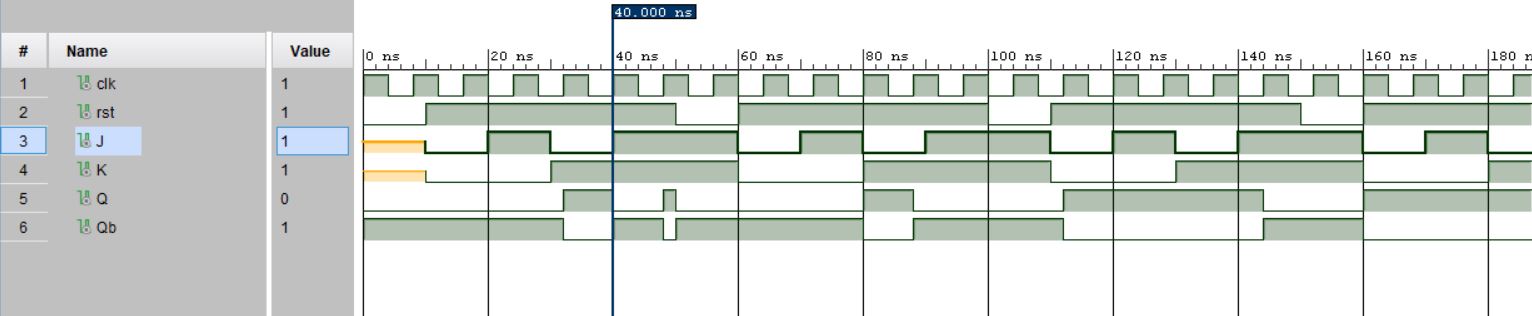
K<='1';

wait for 10ns;

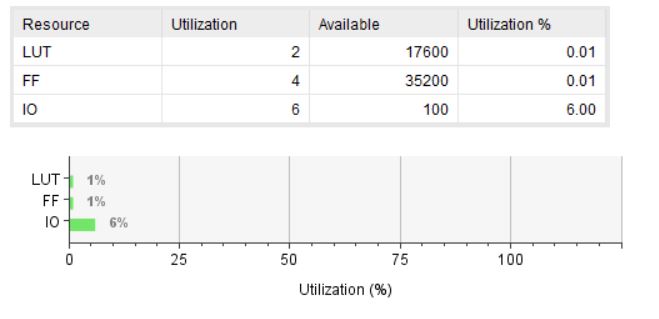
end process;

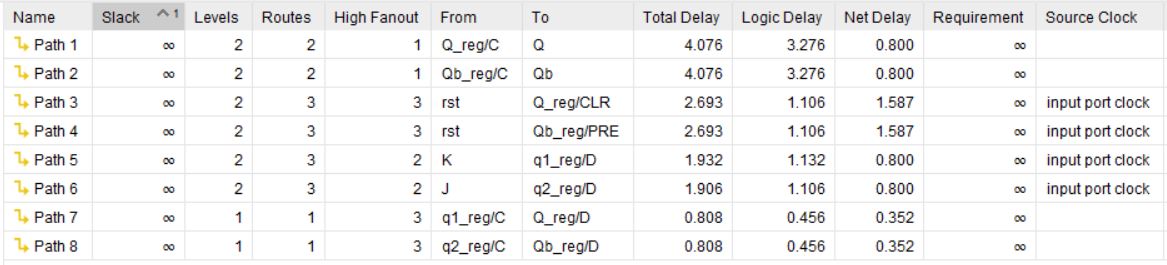
end Behavioral;

**SIMULATION WAVEFORM :**

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**SYNTHESIS SUMMARY:**

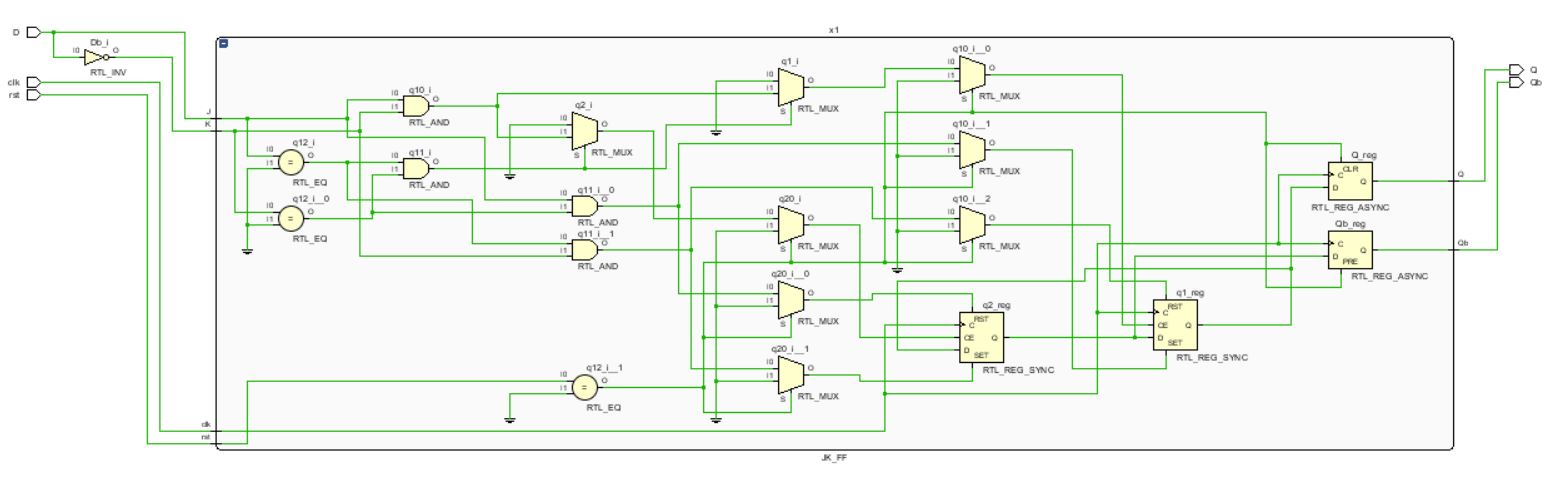
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Maximum Combinational Delay: 4.076nSec

|  |  |  |  |
| --- | --- | --- | --- |
| |  |  |  | | --- | --- | --- | | |  |  | | --- | --- | | |  | | --- | | **Aim:** Write a VHDL Code to implement D Flipflop | | |   **Code:**  library IEEE;  use IEEE.STD\_LOGIC\_1164.ALL;  entity D\_FF is  Port ( clk : in STD\_LOGIC;  rst : in STD\_LOGIC;  D : in STD\_LOGIC;  Q : out STD\_LOGIC;  Qb : out STD\_LOGIC);  end D\_FF;  architecture Behavioral of D\_FF is  component JK\_FF is  Port ( clk : in STD\_LOGIC;  rst : in STD\_LOGIC;  J : in STD\_LOGIC;  K : in STD\_LOGIC;  Q : out STD\_LOGIC;  Qb : out STD\_LOGIC);  end component JK\_FF;  signal Db:STD\_LOGIC;  begin  Db<= not D;  x1:JK\_FF port map(clk,rst,D,Db,Q,Qb);  end Behavioral; |
|  |

**RTL DIAGRAM:**

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**Test bench Code :**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity Tb\_D\_FF is

-- Port ( );

end Tb\_D\_FF;

architecture Behavioral of Tb\_D\_FF is

component D\_FF is

Port ( clk : in STD\_LOGIC;

rst : in STD\_LOGIC;

D : in STD\_LOGIC;

Q : out STD\_LOGIC;

Qb : out STD\_LOGIC);

end component D\_FF;

signal clk,rst,D,Q,Qb:std\_logic;

begin

x1:D\_FF port map(clk,rst,D,Q,Qb);

process

begin

clk<='1';

wait for 5ns;

clk<='0';

wait for 5ns;

end process;

process

begin

rst<='0';

wait for 10ns;

rst<='1';

wait for 50ns;

end process;

Process

begin

D<='0';

wait for 10ns;

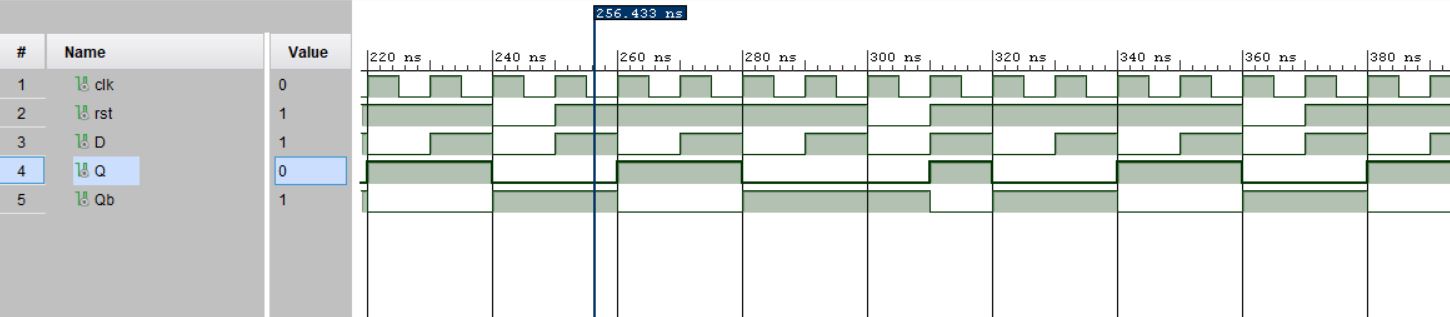
D<='1';

wait for 10ns

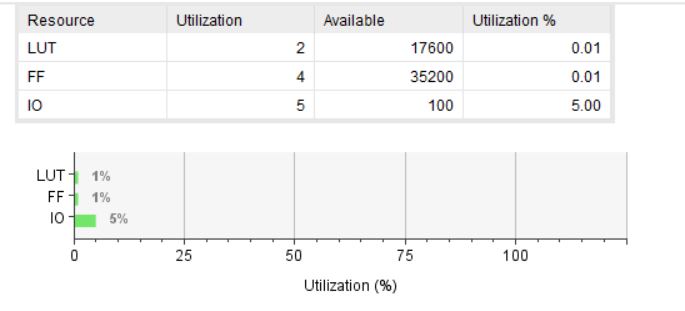
end process;

end Behavioral;

**SIMULATION WAVEFORM :**

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**SYNTHESIS SUMMARY:**

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Maximum Combinational Delay: 4.076nSec